Double Half-Bridge Submodule based Modular Multilevel Converters with Reduced Voltage Sensors

Liu, Chengkai; Deng, Fujin; Wang, Qingsong; Wang, Yanbo; Blaabjerg, Frede; Wang, Zheng

Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2020.3026394

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

Double Half-Bridge Submodule based Modular Multilevel Converters with Reduced Voltage Sensors

Chengkai Liu, Fujin Deng, *Senior Member, IEEE*, Qingsong Wang, *Senior Member, IEEE*, Yanbo Wang, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE* and Zheng Wang, *Senior Member*, *IEEE*

***Abstract*- The half-bridge (HB) submodule (SM) based MMC requires a large number of sensors to measure capacitor voltages. In this letter, a double half-bridge (DHB) SM based MMC is proposed, where each SM consists of two HBs. But only one voltage sensor is equipped in each DHB-SM for capacitor voltage estimation, which is connected between positive poles of two capacitors in the DHB-SM. A capacitor voltage estimation method is also proposed, which can estimate capacitor voltages in the proposed MMC with only a half number of voltage sensors in comparison with HB-SM based MMCs. A DHB-SM based three-phase MMC is simulated with PSCAD/EMTDC and A DHB-SM based single-phase MMC prototype is built in laboratory. Both the simulation and experimental results confirm the effectiveness of the proposed method.**

***Index terms*- Half bridge, modular multilevel converters, voltage sensor, submodule.**

I. INTRODUCTION

The modular multilevel converters (MMCs) have received great interests from both academic and industry due to its advantages like easy construction, flexibility in converter design, excellent output voltage, high efficiency [1-5], etc.

In conventional HB-SM based MMCs, a large number of sensors are equipped to measure the capacitor voltages, where the number of voltage sensor is the same to that of the submodule (SM) [6]. Recently, a number of studies are focused on reducing voltage sensors in MMCs, which can be divided into three categories, including software-based methods, hardware-based methods and fix pattern-based methods.

In software-based methods, the SM capacitor voltages are estimated through the system dynamics along with a number of extra sensors. The individual capacitor voltages can be estimated with weighted recursive least square algorithm [7] or Kalman Filter [8], where extra voltage sensors are equipped to measure the arm voltages. Similarly, an adaptive linear neuron algorithm is used in [9], where the voltages on the arm inductors are measured by extra voltage sensors. In [10], the output voltages of SM groups are measured by sensors, and the capacitor voltages can be obtained when only one SM is activated in the SM group. A capacitor voltage estimation with capacitance self-updating based on grouping measurement is presented in [11], which increases the accuracy of the voltage estimation. Even no extra sensors are applied, the capacitor voltages can be estimated with adaptive observers [12] or Kalman Filters [13]. The main limitations of the software-based methods are: 1) Computational burden is explosively increased along with the increase of number of SMs, which limits its application to MMCs with small number of SMs. 2) High voltage sensors or sensors with high galvanic isolation voltage are required.

In hardware-based methods, extra semiconductor devices are equipped to balance the SM capacitor voltages. A diode-clamp MMC with SM voltage self-balancing ability is presented in [14], where two adjacent capacitors can be paralleled through the clamping diode. To limit the balancing current, small inductors are connected in series with the clamping diodes in a diode-clamp MMC based STATCOM [15] and a diode-clamp MMC based DC transformer [16]. In [17], additional two diodes are used for symmetrical HB-SM to achieve sensorless voltage balance. A semi-full-bridge SM is presented in [18], where two capacitors can be connected in parallel through the conducted insulated gate bipolar transistors (IGBTs). In [19], a reduced series/parallel module are presented for cascaded multilevel converter, which can be configured in series, bypassed or in parallel to balance all capacitor voltages in a sensorless manner. The number of voltage sensors can be reduced by hardware-based methods, which also reduces the communication burden and computational burden in regards of the voltage balancing controls [20]. However, the limitations of the hardware-based methods are evident: 1) The balancing current would be large when the voltage deviation between two paralleled capacitors is large, especially during the startup process, which requires semiconductor devices with big capability. 2) Extra devices not only lead to extra losses but it will also increase the costs.

In fix pattern-based methods, the SMs are switched into a fixed pattern that the power absorbed by each SM is equal. A fix pulse pattern with harmonic elimination is presented in [21], where the stored energy in each SM remains stable. A hierarchical permutation cyclic coding method can evenly distribute the switching gate signals among the SMs [22] and the SM capacitor voltages can be balanced in a wide range of switching frequencies. A Y-Matrix Modulation method is presented in [23], where MMCs can achieve self-voltage balancing without measurements and feedback controls. However, in practical systems, the power losses of SMs can be various due to manufacturing errors [24] or different leakage resistances in valve tower [25]. The fix pattern-based methods cannot ensure an exact voltage balancing.

This work was supported in part by the National Natural Science Foundation of China under Project 61873062 and in part by the Natural Science Foundation of Jiangsu Province under Project BK20180395. *(Corresponding author: Fujin Deng.)*

C. Liu, Q. Wang and Z. Wang are with School of Electrical Engineering, Southeast University, Nanjing 210096, China (e-mail: lckisafish@163.com; qswang@seu.edu.cn; zwang@seu.edu.cn).

F. Deng is with the School of Electrical Engineering, Southeast University, and Jiangsu Key Laboratory of Smart Grid Technology and Equipment, Nanjing 210096, China (e-mail: fdeng@seu.edu.cn).

Y. Wang and F. Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: ywa@et.aau.dk; fbl@et.aau.dk).

This letter proposes a double half-bridge (DHB) SM based MMC, where only a voltage sensor is equipped between positive poles of two capacitors in each DHB-SM. In addition, the corresponding capacitor voltage estimation method is also proposed for each DHB-SM with a simple algorithm. The proposed DHB-SM based MMC only requires a half number of voltage sensors in comparison with the conventional HB-SM based MMC [6].

The rest of letter is organized as follows. The proposed DHB-SM based MMCs and capacitor voltage estimation methods are presented in Section II and Section III, respectively. The simulation and experimental studies are presented in Section IV and Section V, respectively. Finally, the conclusions are drawn in Section VI.

II. Proposed DHB-SM Based MMCs

A single-phase DHB-SM based MMC is shown in Fig. 1(a), which consists of an upper arm and a lower arm. Each arm consists of N identical DHB-SMs and an inductor L_s. Fig. 1(b) shows the i-th (i=1, 2..., N) DHB-SM in the upper arm, which is composed of two HBs (HB$_{i1}$ & HB$_{i2}$) connected in series. The HB$_{ij}$ (j=1, 2) consists of two switches (T_{uij}, T_{lij}) and one capacitor C_{ij}, which are controlled by the switching function S_{ij} as listed in Table I. When S_{ij} =1, T_{uij} is on and T_{lij} is off. Here, the capacitor C_{ij} is inserted into the arm and capacitor voltage u_{cij} is increased with positive arm current and decreased with negative arm current. When S_{ij} =0, T_{uij} is off and T_{lij} is on. The capacitor C_{ij} is bypassed from the arm, and u_{cij} is unchanged.

One thing to mention is that, only one voltage sensor is used between the positive poles of two capacitors in each DHB-SM to estimate capacitor C_{i1}'s voltage and C_{i2}'s voltage, which will be discussed more in Section III.

TABLE I
Switching States of HB$_{ij}$

S_{ij}	T_{uij}	T_{lij}	i_{au}	u_{cij}
1	on	off	Positive	Increase
			Negative	Decrease
0	off	on	Positive	Unchange
			Negative	

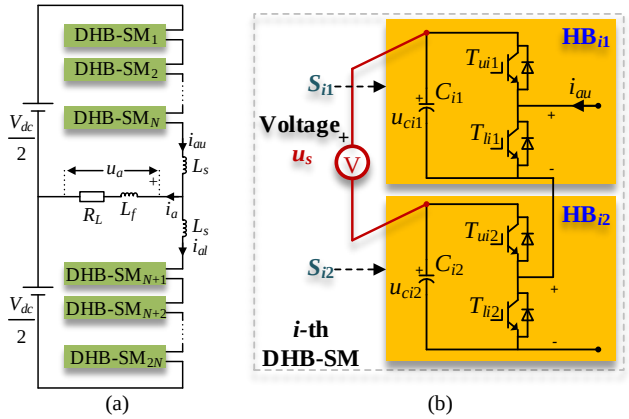


Fig. 1 (a) Single-phase DHB-SM based MMC. (b) Topology of i-th DHB-SM.

TABLE II
Relationship between S_{i2} and u_s

S_{i2}	u_s
1	u_{ci1}
0	u_{ci1}- u_{ci2}

III. Proposed Capacitor Voltage Estimation Method for DHB-SMs Based MMCs

A. Sensor's Measurement Voltage

In the i-th DHB-SM, as shown in Fig. 1(b), only one voltage sensor is equipped to estimate capacitor voltage u_{ci1} and u_{ci2}. The measurement voltage u_s obtained from the sensor depends on the S_{i2} corresponding to HB$_{i2}$, as listed in Table II.

1) S_{i2}=1: the sensor is connected in parallel with the C_{i1}, as depicted in Fig. 2(a). Here, $u_s = u_{ci1}$.
2) S_{i2}=0: the negative poles of C_1 and C_2 are connected together, as depicted in Fig. 2(b). Here, the u_s equals to the voltage deviation Δu_{ci} between C_{i1}'s voltage u_{ci1} and C_{i2}'s voltage u_{ci2}, as u_s=Δu_{ci}=u_{ci1}-u_{ci2}.

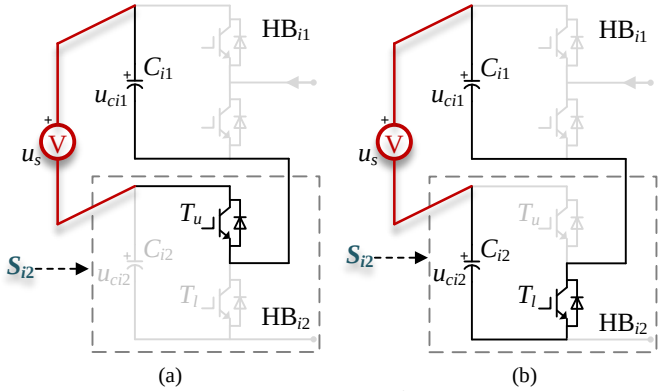


Fig. 2. Sensor voltage u_s corresponding to S_{i2} of HB$_{i2}$. (a) S_{i2} = 1. (b) S_{i2} = 0.

B. Proposed Capacitor Voltage Estimation Method

Based on the above analysis, a capacitor voltage estimation method is proposed. Fig. 3 shows the proposed capacitor voltage estimation method for the i-th DHB-SM in the upper arm. In Fig. 3(a), the SM individual voltage balancing control method [26] including voltage balancing control (VBC) and voltage average control (VAC) is employed for the MMC. With the ac-side voltage reference u_a^*, estimated capacitor voltage $\hat{u}_{ci1}$ and $\hat{u}_{ci2}$, and average capacitor voltage u_{c_ave} in the phase, the reference signals y_{i1} and y_{i2} can be produced and compared with two carriers to generate the switching functions S_{i1} and S_{i2} for the HB$_{i1}$ and HB$_{i2}$ in the i-th DHB-SM, respectively, which can ensure the capacitor voltage balancing in the MMC and it is close to the rated SM capacitor voltage u_{c0} as

$$u_{c0} = V_{dc}/(2N). \tag{1}$$

In Fig. 3, the average capacitor voltage u_{c_ave} is

$$u_{c\_ave} = \sum_{i=1}^{2N} (\hat{u}_{ci1} + \hat{u}_{ci2}) / (4N) \tag{2}$$

In the MMC, the phase-shifted carrier (PSC) based pulse width modulation (PWM) technique is adopted. The 2N isosceles triangle carriers with the phase-shifted angle of π/N are employed for SMs in the upper arm, where the carrier period is T_s and angular frequency is ω_s=$2\pi/T_s$. In Fig. 3(a), the initial phase angle of carrier W_{i2} for the HB$_{i2}$ in the i-th DHB-SM is

$$\theta_{i2} = (2i\text{-}1) \cdot \pi/N. \tag{3}$$

Fig. 3(b) shows the detailed modulation for the HB$_{i2}$. The S_{i2} is generated based on the y_{i2} and W_{i2} as

- S_{i2}=1 if y_{i2}>W_{i2}

- S_{i2}=0 if y_{i2}<W_{i2}

As a result, Table III can be easily obtained as

- S_{i2}=1 at the valley of W_{i2} and this instant is

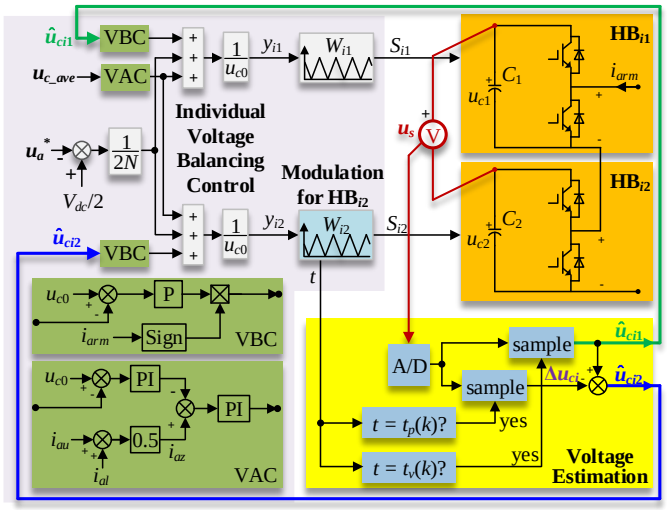
$$t_v(k)=\frac{\theta_{i2}}{\omega_s}+(k+\frac{1}{2})\cdot T_s=(\frac{2i-1}{2N}+k+\frac{1}{2})\cdot T_s,\quad (k=0,1,2...)\ .\ (4)$$

- S_{i2}=0 at the peak of W_{i2} and this instant is

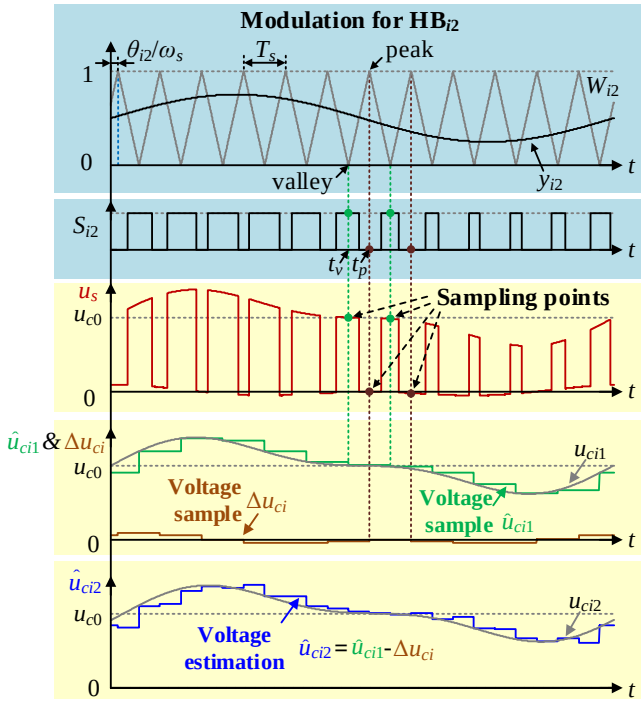
$$t_p(k)=\frac{\theta_{i2}}{\omega_s}+k\cdot T_s=(\frac{2i-1}{2N}+k)\cdot T_s,\quad (k=0,1,2...)\ .\qquad (5)$$

TABLE III
Relationship among t, W_{i2} and S_{i2}

t	W_{i2}	S_{i2}
$t_v(k)$=[(2i-1)/(2N)+k+1/2]·T_s	Valley	1
$t_p(k)$=[(2i-1)/(2N)+k]·T_s	Peak	0



(a)



(b)

Fig. 3. Proposed capacitor voltage estimation method. (a) Capacitor voltage estimation for the i-th DHB-SM. (b) Proposed synchronous sampling.

Based on Tables II and III, the capacitor voltage u_{ci1} of C_{i1} and u_{ci2} of C_{i2} can be sampled and estimated from the sensor voltage u_s, where the sampling of the sensor voltage u_s and the estimation of capacitor voltage are synchronized with the carrier W_{i2} for HB$_{i2}$, as follows.

1) Estimation of voltage $\hat{u}_{ci1}$ for C_{i1}

$\hat{u}_{ci1}$ is periodically sampled from sensor voltage u_s at the time $t_v(k)$ with period of T_s, as shown in Fig. 3(b), given as

$$\hat{u}_{ci1}=u_s(t)\big|_{t=t_v(k)} \qquad (6)$$

2) Estimation of voltage $\hat{u}_{ci2}$ for C_{i2}

The voltage deviation Δu_c is periodically sampled from sensor voltage u_s at the time $t_p(k)$ with period of T_s, as shown in Fig. 3(b), as

$$\Delta u_{ci}=u_s(t)\big|_{t=t_p(k)}\ . \qquad (7)$$

As a result, the $\hat{u}_{ci2}$ can be estimated as

$$\hat{u}_{ci2}=\hat{u}_{ci1}-\Delta u_{ci}\ . \qquad (8)$$

IV. Simulation Studies

To verify the effectiveness of the proposed method, a three-phase DHB-SM based MMC (12 DHB-SMs per arm) is simulated with PSCAD/EMTDC, while a three-phase HB-SM based MMC (24 HB-SMs per arm) is also simulated for comparison. The diagram of the simulated system is shown in Fig. 4 and the system parameters are listed in TABLE IV. Initially, the active power P and the reactive power Q are regulated at 18 MW and 0 MVar, respectively. At 2.5 s, P is reduced to 9 MW in a step and Q is not changed.

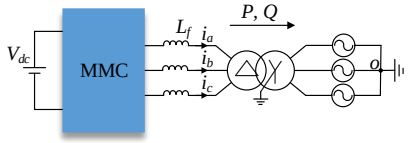


Fig. 4. Diagram of the simulated system.

TABLE IV
Parameters for Simulated System

Parameter	Value
Rated power (MW)	20
DC link voltage V_{dc} (kV)	24
Rated frequency (Hz)	50
Grid line-to-line voltage	33 kV
Transformer voltage rating	12 kV/33 kV
Rated capacitor voltage u_{c0} (kV)	1
SM capacitance (mF)	15
Arm inductance L_s (mH)	4
Filter inductance L_f (mH)	1
Carrier frequency 1/T_s (Hz)	110

A. Case I: DHB-SM based MMC

Figs. 5~7 show the performance of the proposed DHB-SM based MMC. Fig. 5 shows the ac-side current i_a, i_b and i_c. Fig. 6(a) shows the estimated capacitor voltage $\hat{u}_{c11}$ and capacitor voltage u_{c11} for C_{11} in HB$_{11}$ of DHB-SM$_1$ in upper arm of phase A. Fig. 6(b) shows the estimated capacitor voltage $\hat{u}_{c12}$ and capacitor voltages u_{c12} for C_{12} in HB$_{12}$ of DHB-SM$_1$. It can be observed that the estimated $\hat{u}_{c11}$ and $\hat{u}_{c12}$ are coinciding with u_{c11} and u_{c12}, respectively.

Fig. 7(a) shows the capacitor voltages in DHB-SM$_1$~DHB-SM$_{12}$ in upper arm of phase A, while Fig. 7(b) shows the capacitor voltages in DHB-SM$_{13}$~DHB-SM$_{24}$ in

lower arm of phase A. It can be observed that the capacitor voltages can be well balanced at such a low switching frequency.

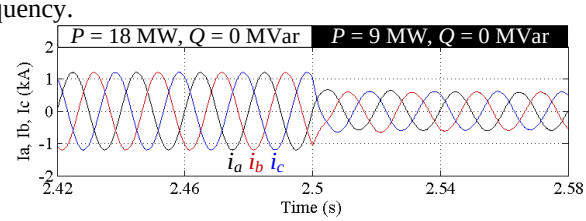


Fig. 5. AC-side current i_a, i_b and i_c of DHB-SM based MMC.

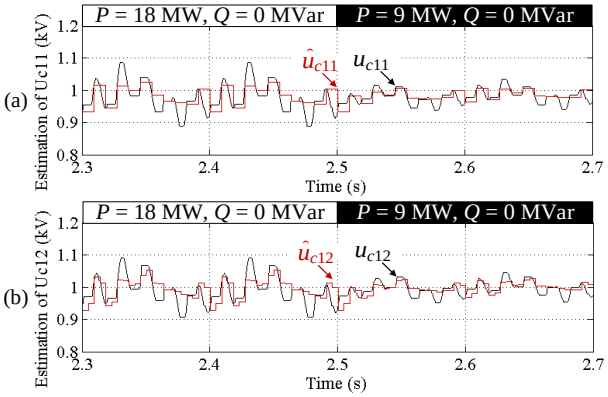


Fig. 6. Voltage estimation. (a) Estimated voltage $\hat{u}_{c11}$ and capacitor voltage u_{c11} for HB_{11} in DHB-SM_1 in upper arm of phase A. (b) Estimated voltage $\hat{u}_{c12}$ and capacitor voltage u_{c12} for HB_{12} in DHB-SM_1 in upper arm of phase A.

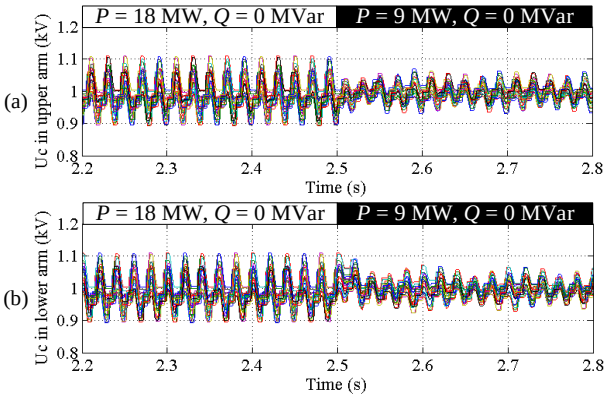


Fig. 7. Capacitor voltages in DHB-SM based MMC. (a) DHB-SM_1~DHB-SM_{12} in upper arm of phase A. (b) DHB-SM_{13}~DHB-SM_{24} in lower arm of phase A.

B. Case II: HB-SM based MMC

Fig. 8 shows the ac-side current i_a, i_b and i_c of the HB-SM based MMC. In comparison with Fig. 5, the current performance of the DHB-SM based MMC is almost the same to that of the HB-SM based MMC.

Fig. 9(a) shows the capacitor voltages in HB-SM_1~HB-SM_{24} in upper arm of phase A. Fig. 9(b) shows the capacitor voltages in HB-SM_{25}~HB-SM_{48} in lower arm of phase A. In comparison with Fig. 7, the capacitor voltage performance of the proposed DHB-SM based MMC is also similar to that of the HB-SM based MMC.

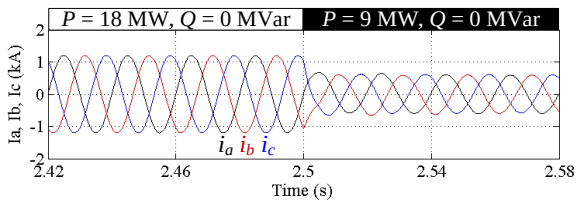


Fig. 8. AC-side current i_a, i_b and i_c of HB-SM based MMC.

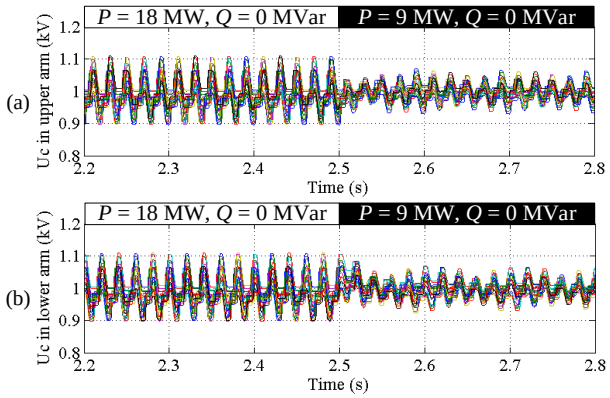


Fig. 9. Capacitor voltages in HB-SM based MMC. (a) HB-SM_1~HB-SM_{24} in upper arm of phase A. (b) HB-SM_{25}~HB-SM_{48} in lower arm of phase A.

V. Experimental Studies

A single-phase DHB-SM based MMC prototype, as shown in Fig. 1(a), is built in the laboratory. Fig. 10 shows a photo of the experimental setup. The dc power supply SGA600/8 supports the dc link of the MMC. The IXFK48N36P is used as the switch/diode in each DHB-SM. The ac-side current control and VAC are implemented in a digital signal processor controller TMS32F28335. The voltage estimation, VBC and PSC-PWM are implemented in the FPGA device XC6SLX25. The system parameters are listed in TABLE V.

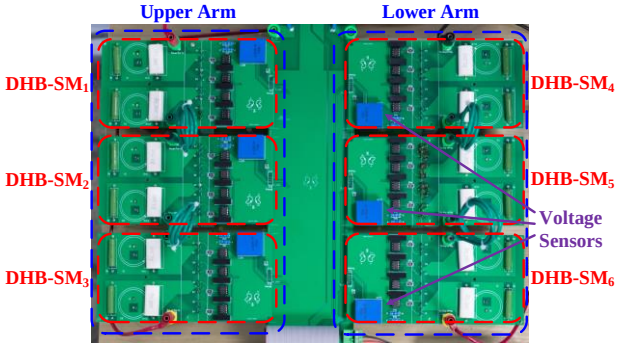


Fig. 10. Photo of the experimental setup.

TABLE V
Parameters for Experimental System

Parameter	Value
DC link voltage V_{dc} (V)	300
Rated frequency (Hz)	50
Number of DHB-SM per arm N	3
Rated capacitor voltage u_{c0} (V)	50
SM capacitance (mF)	3.9
Arm inductance L_s (mH)	1.8
Filter inductance L_f (mH)	1.8
Load resistance R_L (Ω)	10
Carrier frequency $1/T_s$ (Hz)	400

Figs. 11~14 show the performance of the proposed MMC, where the ac-side current i_a is changed from 9 A to 4.5 A in a step. Fig. 11 shows i_a, upper arm current i_{au} and lower arm current i_{al}.

Fig. 12 shows the estimated capacitor voltage $\hat{u}_{c11}$ and measured capacitor voltages u_{c11} for C_{11} in HB_{11} of DHB-SM_1, as well as the estimated capacitor voltage $\hat{u}_{c12}$ and measured capacitor voltages u_{c12} for C_{12} in HB_{12} of DHB-SM_1, where the

estimated capacitor voltages are output by digital-analog converter and recorded by the oscilloscope. It can be observed that the estimated $\hat{u}_{c11}$ and $\hat{u}_{c12}$ are coinciding with the measured u_{c11} and u_{c12}, respectively.

Fig. 13 shows the measured capacitor voltages u_{c11} and u_{c12} in DHB-SM$_1$ and measured capacitor voltages u_{c21} and u_{c22} in DHB-SM$_2$ in upper arm. Fig. 14 shows measured capacitor voltages u_{c41} and u_{c42} in DHB-SM$_4$ and measured capacitor voltages u_{c51} and u_{c52} in DHB-SM$_5$ in lower arm. It can be observed that the capacitor voltages in the proposed MMC can be well balanced with the estimated capacitor voltages in the proposed method.

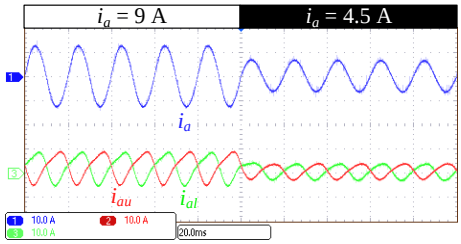


Fig. 11. AC-side current i_a, upper arm current i_{au} and lower arm current i_{al}.

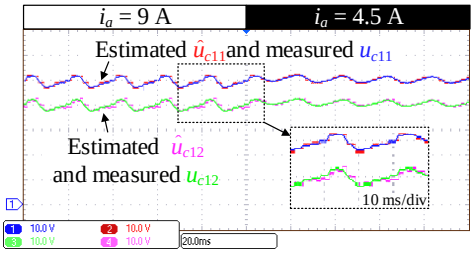


Fig. 12. Estimated voltage $\hat{u}_{c11}$ and measured voltage u_{c11} for HB$_{11}$ in DHB-SM$_1$ in upper arm. Estimated voltage $\hat{u}_{c12}$ and measured voltage u_{c12} for HB$_{12}$ in DHB-SM$_1$ in upper arm.

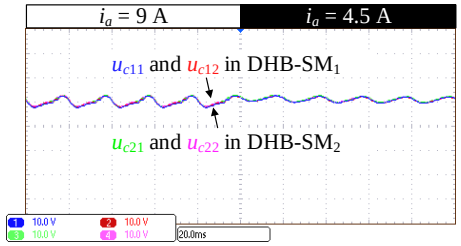


Fig. 13. Capacitor voltages for DHB-SM$_1$ and DHB-SM$_2$ in upper arm.

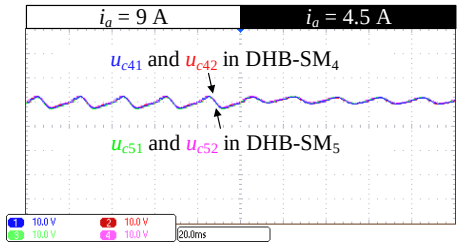


Fig. 14. Capacitor voltages for DHB-SM$_4$ and DHB-SM$_5$ in lower arm.

VI. Conclusions

This letter proposes a DHB-SM for MMCs, where only one voltage sensor is equipped in each DHB-SM to measure the voltage between positive poles of two capacitors. The voltage estimation method is also proposed based on the sampled voltages at peak and valley of the carriers. The proposed MMC reduces the number of voltage sensors to half in comparison with the conventional HB-SM based MMC. The simulation and experimental results confirm the effectiveness of the proposed DHB-SM based MMC and capacitor voltage estimation method.

References

[1] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4-17, Jan. 2015.

[2] A. Nami, J. Liang, F. Dijkhuizen and G. D. Demetriades, "Modular Multilevel Converters for HVDC Applications: Review on Converter Cells and Functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18-36, Jan. 2015.

[3] F. Deng, Y. Lv, C. Liu, Q. Heng, Q. Yu and J. Zhao, "Overview on Submodule Topologies, Modeling, Modulation, Control Schemes, Fault Diagnosis and Tolerant Control Strategies of Modular Multilevel Converters," *Chin. J. Elect. Eng*., vol. 6, no. 1, pp. 1-21, March 2020.

[4] C. Liu *et al*., "Fault Localization Strategy for Modular Multilevel Converters Under Submodule Lower Switch Open-Circuit Fault," *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 5190-5204, May 2020.

[5] F. Deng, Z. Chen, M. R. Khan and R. Zhu, "Fault Detection and Localization Method for Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2721-2732, May 2015.

[6] Q. Tu, Z. Xu and L. Xu, "Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters," *IEEE Trans. Power Del.*, vol. 26, no. 3, pp. 2009-2017, July 2011.

[7] O. S. M. Abushafa, S. M. Gadoue, M. S. A. Dahidah, D. J. Atkinson and P. Missailidis, "Capacitor Voltage Estimation Scheme With Reduced Number of Sensors for Modular Multilevel Converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 4, pp. 2086-2097, Dec. 2018.

[8] O. S. H. M. Abushafa, M. S. A. Dahidah, S. M. Gadoue and D. J. Atkinson, "Submodule Voltage Estimation Scheme in Modular Multilevel Converters with Reduced Voltage Sensors Based on Kalman Filter Approach," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp. 7025-7035, Sept. 2018.

[9] M. Abdelsalam, M. Marei, S. Tennakoon and A. Griffiths, "Capacitor voltage balancing strategy based on sub-module capacitor voltage estimation for modular multilevel converters," *CSEE J. Power and Energy Sys.*, vol. 2, no. 1, pp. 65-73, March 2016.

[10] R. Picas, J. Zaragoza, J. Pou, S. Ceballos and J. Balcells, "New Measuring Technique for Reducing the Number of Voltage Sensors in Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 177-187, Jan. 2016.

[11] L. Peng and Z. Wang, "Grouping Capacitor Voltage Estimation and Fault Diagnosis with Capacitance Self-Updating in Modular Multilevel Converters," *IEEE Trans. Power Electron.*, to be published, 2020.

[12] H. Nademi, A. Das and L. E. Norum, "Modular Multilevel Converter With an Adaptive Observer of Capacitor Voltages," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 235-248, Jan. 2015.

[13] M. D. Islam, R. Razzaghi and B. Bahrani, "Arm-Sensorless Sub-Module Voltage Estimation and Balancing of Modular Multilevel Converters," *IEEE Tran. Power Del.*, vol. 35, no. 2, pp. 957-967, April 2020.

[14] C. Gao, X. Jiang, Y. Li, Z. Chen and J. Liu, "A DC-Link Voltage Self-Balance Method for a Diode-Clamped Modular Multilevel Converter With Minimum Number of Voltage Sensors," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2125-2139, May 2013.

[15] X. Liu, J. Lv, C. Gao, Z. Chen and S. Chen, "A Novel STATCOM Based on Diode-Clamped Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5964-5977, Aug. 2017.

[16] T. Zheng *et al*., "A Novel High-Voltage DC Transformer Based on Diode-Clamped Modular Multilevel Converters with Voltage Self-Balancing Capability," *IEEE Trans. Ind. Electron.*, to be published, 2020.

[17] J. Fang, Z. Li and S. Goetz, "Multilevel Converters with Symmetrical Half-Bridge Submodules and Sensorless Voltage Balance," *IEEE Trans. Power Electron.*, to be published, 2020.

[18] S. Heinig *et al*., "Implications of Capacitor Voltage Imbalance on the Operation of the Semi-Full-Bridge Submodule," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9520-9535, Oct. 2019.

[19] Z. Li, J. K. Motwani, Z. Zeng, S. Lukic, A. V. Peterchev and S. Goetz, "A Reduced Series/Parallel Module for Cascade Multilevel Static

Compensators Supporting Sensorless Balancing," *IEEE Trans. Ind. Electron*., to be published, 2020.

[20] L. Mathe, P. D. Burlacu and R. Teodorescu, "Control of a Modular Multilevel Converter With Reduced Internal Data Exchange," *IEEE Trans. Ind. Informat.*, vol. 13, no. 1, pp. 248-257, Feb. 2017.

[21] K. Ilves, A. Antonopoulos, S. Norrga and H. Nee, "A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482-3494, Aug. 2012.

[22] A. Ghazanfari and Y. A. I. Mohamed, "A Hierarchical Permutation Cyclic Coding Strategy for Sensorless Capacitor Voltage Balancing in Modular Multilevel Converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 576-588, June 2016.

[23] Y. Liu and F. Z. Peng, "A Modular Multilevel Converter with Self Voltage Balancing -Part II: Y-Matrix Modulation," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 8, no. 2, pp. 1126-1133, June 2020.

[24] F. Deng *et al*., "Power Losses Control for Modular Multilevel Converters Under Capacitor Deterioration," *IEEE J. Emerg. Sel. Topics Power Electron*., to be published, 2020.

[25] Y. Hu, Z. Chang and Y. Qiu, "Analysis of MMC Value Tower Waterway on Static Voltage Balancing of Submodule," *IEEE Trans. Power Electron*., vol. 53, no. 7, pp. 125-128, July 2019.

[26] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737-1746, July 2009.